

Enrollment No./Seat No.:

GUJARAT TECHNOLOGICAL UNIVERSITY
Bachelor of Engineering - SEMESTER - III EXAMINATION - WINTER 2025

Subject Code: BE03000071

Date: 15-12-2025

Subject Name: Digital Fundamentals

Time: 10:30 AM TO 01:00 PM

Total Marks: 70

Instructions

- 1. Attempt all questions.**
- 2. Make suitable assumptions wherever necessary.**
- 3. Figures to the right indicate full marks.**
- 4. Simple and non-programmable scientific calculators are allowed.**

	Marks
Q.1 (a) Differentiate between Binary code and Gray code representation.	03
(b) Simplify the given Boolean expression $F = xy'z' + yz + xz'$ and draw the final circuit using basic logic gates.	04
(c) Explain the following terms in context of digital ICs: Threshold voltage, Propagation delay, Noise Margin, Power dissipation, Fan in, Fan out, Speed power products.	07
Q.2 (a) Differentiate between Demultiplexer and Decoder.	03
(b) Explain the SOP and POS representations of Boolean expressions with suitable examples.	04
(c) Simplify the following Boolean function using K-map and implement it using NAND gates: $F(A,B,C,D) = \sum m(0,1, 3, 4, 7, 9, 11) + d(8, 10, 15)$.	07
OR	
(c) Simplify the Boolean function $F(A,B,C,D) = \sum m(0,1,6,7,8,9,13,14,15)$ using the Quine–McCluskey (Tabulation) method and draw its logic circuit.	07
Q.3 (a) Describe the Look-Ahead Carry Adder unit.	03
(b) Implement the following Boolean functions with a 8 x 1 multiplexer. $F(w, x, y, z) = \sum(1, 3, 4, 5, 12, 13, 15)$	04
(c) Explain the D flip flop with its characteristics table and excitation table.	07
OR	
(a) Define Race Around Condition in JK flip flop.	03
(b) Differentiate between combinational circuit and sequential circuit. Also list the possible applications of it.	04
(c) Explain the 2-bit magnitude comparator with a suitable combinational circuit diagram.	07
Q.4 (a) Describe how D flip-flop is converted into T flip-flop.	03

- (b) Differentiate between registers and counters based on their structure and functionality. 04
- (c) Design mod-5 synchronous counter using JK flip flop. 07

OR

- (a) Define clock triggering mechanism for sequential circuit. 03
- (b) Compare the Synchronous and Asynchronous counters. 04
- (c) Write a brief note on 4-bit parallel in, serial out shift register with its block diagram. 07

- Q.5**
- (a) Describe the Content addressable memory. 03
 - (b) Explain the internal representation of 2k x 8 ROM chip. 04
 - (c) A combinational logic circuit is defined by the functions: $F1 = \sum (0,1,2,4)$ and $F2 = \sum (0, 5, 6,7)$. Implement the circuit with a PLA having three inputs, four product terms and two outputs. 07

OR

- (a) Explain the following terms for memory: Data line, Address line, Control line 03
- (b) Implement the following Boolean expressions using a PROM. 04
 $f1(a, b, c) = \sum m(0, 2, 3, 5, 6)$
 $f2(a, b, c) = \sum m(1, 2, 4, 7)$
- (c) Explain the working principles of Programmable Logic Devices (PROM, PLA, and PAL) with suitable comparisons. 07
