Enrollment No./Seat No.:

GUJARAT TECHNOLOGICAL UNIVERSITY

Bachelor of Engineering - SEMESTER - V EXAMINATION - WINTER 2025

Subject Code: 3154704 **Date: 27-11-2025**

Subject Name: VLSI Technology and Design

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Write VHDL program for 1-bit full adder.	**03**
	(b)	Design CMOS SR latch circuit based on NOR gate.	**04**
	(c)	Explain Fabrication of n-MOSFET with neat sketch.	**07**
Q.2	**(a)**	Enlist different types of MOSFET capacitance.	**03**
	(b)	Compare different load inverters.	**04**
	(c)	Draw i/p and o/p waveform during high to low transition of o/p for CMOS inverter and derive expression for t_{PHL} using differential equation method.	**07**
		OR	
	(c)	Explain interconnect delay analysis using Elmore Delay model.	**07**
Q.3	**(a)**	Why is the size of PMOS transistor chosen to be 2.5 times of an NMOS transistor?	**03**
	(b)	Construct D latch using CMOS inverters and Transmission Gates.	**04**
	(c)	Derive MOSFET current -voltage characteristics using gradual channel approximation.	**07**
		OR	
	(a)	Derive switching power dissipation equation of CMOS inverter with idea step input.	**03**
	(b)	Draw CMOS ring oscillator and its out waveform. Write generated frequency equation.	**04**
	(c)	Explain MOS System under External Bias with neat sketch of cross sectional view and energy band diagram and derive depletion region depth equation.	**07**
Q.4	**(a)**	Compare constant field and constant voltage scaling.	**03**
	(b)	Draw resistive load inverter. Derive V_{OL} and V_{IL} critical voltages equation of resistive load inverter.	**04**
	(c)	Write a short note on CMOS Transmission gate.	**07**
		OR	
	(a)	Implement following Boolean expression using CMOS inverter Z= (A(D+E)+BC)'	**03**

	(b)	Draw CMOS inverter with leads name of pMOS and nMOS transistors. Derive V_{IL} critical Voltage equation of CMOS inverter	**04**
	(c)	Draw ASIC design flow chart and write HDL program to implement 4x1 multiplexer using verilog hardware description language.	**07**
Q.5	**(a)**	Draw VLSI design flow Y chart.	**03**
	(b)	Implement 2 inputs NOR and NAND gates using depletion load inverter.	**04**
	(c)	Draw CMOS implementation of D latch with two inverter and two CMOS TG gates.	**07**

OR

	(a)	Define Concept of Regularity, Modularity, and Locality.	**03**
	(b)	Explain ASIC design flow.	**04**
	(c)	Derive the equation for propagation delay of output signal during high to low transition of output of CMOS inverter circuit with C_{load} as load capacitance.	**07**

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