

**GUJARAT TECHNOLOGICAL UNIVERSITY****BE- SEMESTER-III EXAMINATION – WINTER 2025****Subject Code:3132003****Date:15-12-2025****Subject Name: Design Concepts in Basic Electronics****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

|  | <b>Marks</b> |
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| <b>Q.1</b> (a) Explain the Positive Biased Clipper circuit with figure.  | <b>03</b>    |
| (b) Differentiate between analog system and digital system.  | <b>04</b>    |
| (c) Explain 8×1 Multiplexer with circuit diagram.  | <b>07</b>    |
| <b>Q.2</b> (a) Convert :   | <b>03</b>    |
| (1). $(0.6875)_{10} = (\text{_____})_2$  |              |
| (2). $(673.124)_8 = (\text{_____})_2$  |              |
| (3). $(10110001101011.111100000110)_2 = (\text{___})_8$  |              |
| (b) Draw the logic diagram and state truth table for J-K -flip flop.   | <b>04</b>    |
| (c) Simplify the Boolean function $F(A,B,C,D) = \Sigma(0,1,2,5,8,9,10)$ in sum of products using k-map with GATE implementation and truth table.   | <b>07</b>    |
| <b>OR</b>  |              |
| (c) Explain significance of digital system with block diagram.   | <b>07</b>    |
| <b>Q.3</b> (a) Design and explain half adder combinational logic circuit.  | <b>03</b>    |
| (b) Explain forward bias V-I characteristics of PN junction diode.   | <b>04</b>    |
| (c) Explain with neat diagram working of 4-bit bidirectional shift register with parallel load.  | <b>07</b>    |
| <b>OR</b>  |              |
| <b>Q.3</b> (a) Briefly explain intrinsic material and extrinsic material.  | <b>03</b>    |
| (b) Construct and explain working of 3-bit decoder.  | <b>04</b>    |
| (c) Explain input and output characteristics of CB configuration of transistor.  | <b>07</b>    |
| <b>Q.4</b> (a) Explain Voltage Tripler circuits with circuit diagram.  | <b>03</b>    |
| (b) Design 1-Bit magnitude comparator.   | <b>04</b>    |
| (c) Design 3bit up-down synchronous counters with help of T-flip flop.   | <b>07</b>    |
| <b>OR</b>  |              |
| <b>Q.4</b> (a) Explain Capacitor Filter for bridge rectifier with circuit diagram and waveforms.   | <b>03</b>    |
| (b) Explain the input output characteristics of N-P-N transistor in CE configuration.  | <b>04</b>    |
| (c) Derive the following parameter for full wave bridge rectifier.<br>1) RMS load current, 2) RMS load Voltage, 3) Average load Current, 4) PIV 5) Average load Voltage, 6) Ripple Factor. | <b>07</b>    |
| <b>Q.5</b> (a) What are the applications of Transistor-Transistor Logic (TTL) circuits?  | <b>03</b>    |
| (b) Explain 3-bit Asynchronous Counter in detail.  | <b>04</b>    |
| (c) Explain emitter feedback bias for transistor.  | <b>07</b>    |
| <b>OR</b>  |              |
| <b>Q.5</b> (a) Prove $(A + B)(A + C) = A + BC$ using Boolean Algebra.  | <b>03</b>    |
| (b) Briefly explain min-terms and max-terms with suitable example.   | <b>04</b>    |
| (c) Explain error detection using parity bit.  | <b>07</b>    |

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