

GUJARAT TECHNOLOGICAL UNIVERSITY**BE- SEMESTER-III EXAMINATION – WINTER 2025****Subject Code:3130704****Date:22-12-2025****Subject Name: Digital Fundamentals****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

		MARKS
Q.1	(a) List out various logic families. Also list characteristics of digital IC.	03
	(b) Convert the decimal number 225.225 to octal and hexadecimal.	04
	(c) Implement AND, OR, EX-OR gates using NAND & NOR gates.	07
Q.2	(a) Draw the logic diagram of 1-digit BCD adder.	03
	(b) State and prove De-Morgan's theorems using truth-tables.	04
	(c) Design 3-bit even parity generator circuit.	07
OR		
	(c) Design full adder circuit using decoder and multiplexer.	07
Q.3	(a) Design half subtractor logic circuit.	03
	(b) Implement D flip flop using JK flip flop.	04
	(c) Design 2 - Bit Magnitude Comparator.	07
OR		
Q.3	(a) Differentiate synchronous counter and asynchronous counter.	03
	(b) Draw & explain in brief the logic diagram of 4-bit bidirectional shift register.	04
	(c) Design a Combinational circuit that convert Binary to BCD code converter.	07
Q.4	(a) Explain S-R clocked flip flop.	03
	(b) Explain the specification of D/A converter.	04
	(c) Design mod-6 asynchronous counter using T flip flop.	07
OR		
Q.4	(a) List out and explain any one application of the register.	03
	(b) Design 4 X 16 decoder using two 3 X 8 decoders.	04
	(c) Design a 3-bit synchronous up counter using JK flip-flops.	07
Q.5	(a) Compare SRAM with DRAM.	03
	(b) Draw & explain the block diagram of ALU.	04
	(c) Write a short note on FPGA.	07
OR		
Q.5	(a) Explain classification of Memories.	03
	(b) Explain R-2R ladder type D/A converter.	04
	(c) Write a short note on ROM & its types.	07
