Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III EXAMINATION – WINTER 2025

Subject Code:3130306 Date:22-12-2025

Subject Name: Fundamentals of Digital Electronics

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Define Digital System and Give the basic difference between Analog and Digital Systems.	**03**
	(b)	Perform the following: (i) Subtract the decimal numbers 3570-2100 using 10's Complement method. (ii) Convert the Octal number 37.45 into Binary number.	**04**
	(c)	Explain all the Basic Logic Gates (AOI), Universal Logic Gates and Exclusive Logic Gates in detail with Truth Tables.	**07**
Q.2	**(a)**	Obtain the truth table of the logical expression: F(A,B,C) = A.B+A.B'+B'.C	**03**
	(b)	Demonstrate the below given properties of Boolean algebra: i) Commutative Property ii) Associative Property iii) Distributive Property	**04**
	(c)	Design & explain Half-Adder Circuit in details with NAND & NOR implementation.	**07**
		OR	
	(c)	Design & explain Half-Subtractor Circuit in details with NAND & NOR implementation.	**07**
Q.3	**(a)**	Find the Minterms of the logical expression F(A,B,C,D) = D(A'+B)+B'D	**03**
	(b)	Describe the Programmable Logic Array (PLA) in brief.	**04**
	(c)	Implement 4*1 MUX using below given logical expression by taking variable X & Y as a select input. F(X,Y,Z) = ∑ m (0,1,4,6,7)	**07**
		OR	
Q.3	**(a)**	Write the canonical SOP form of the logical expression F(A,B,C)=∑ m (0,1,3,4).	**03**
	(b)	Describe the Programmable ROM (PROM) in brief.	**04**
	(c)	Design & explain the Binary to Gray code converter in detail.	**07**
Q.4	**(a)**	Draw the logic diagram of J-K Flip-Flop using NAND gate with truth table.	**03**
	(b)	Simplify the below given logical expression F(A,B,C,D) = A'+ B.C + (C.D)' using De Morgan's theorem.	**04**
	(c)	Implement the J-K Flip-Flop using S-R Flip-Flop with necessary tables and diagrams.	**07**
		OR	
Q.4	**(a)**	Draw the Symbol of Edged triggered D and T type Flip-Flop with their truth tables.	**03**
	(b)	Implement the logical expression F(X,Y,Z) = XY+X'Y'+Y'Z using AND, OR and NOT gate.	**04**
	(c)	Describe the Mealy & Moore model for sequential circuits.	**07**
Q.5	**(a)**	Give the difference between Asynchronous and Synchronous counters.	**03**
	(b)	Draw the logic diagram of 2*4 Decoder with truth table and logical expression.	**04**

	(c)	Design and explain the Serial-In, Serial-Out (SISO) and Serial-In, Parallel-Out (SIPO) Shift Registers in detail.	**07**

OR

Q.5	**(a)**	Draw the logic diagram of 4-bit Ring Counter.	**03**
	(b)	Design the Parallel-Adder Circuit and explain in brief.	**04**
	©	Design and explain the BCD Counter (Decade Counter) using Negative Edge-triggered J-K Flip-flops.	**07**

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