Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–VII (NEW) EXAMINATION – WINTER 2024

Subject Code:3172420 Date:16-12-2024

Subject Name: FPGA in Power Electronics Applications

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Explain difference between combinational logic and sequential logic.	**03**
	(b)	Explain basic architecture of computer.	**04**
	(c)	Explain D-Latch and D-Flip flop in detail.	**07**
Q.2	**(a)**	Explain difference between Signal and Variable.	**03**
	(b)	Explain data attributes with example.	**04**
	(c)	Explain Finite state machines in detail.	**07**
		OR	
	(c)	Explain top-down design approch in detail.	**07**
Q.3	**(a)**	Explain association connectivity in port map.	**03**
	(b)	Explain WHILE-LOOP and FOR-LOOP statement in VHDL	**04**
	(c)	Explain data flow modeling with example.	**07**
		OR	
Q.3	**(a)**	Explain signal attributes with example.	**03**
	(b)	Describe inertial delay model in brief.	**04**
	(c)	Explain behavioral modeling with example.	**07**
Q.4	**(a)**	Write a VHDL code for half adder.	**03**
	(b)	Write a VHDL code to implement 4-bit counter.	**04**
	(c)	Explain predefined operators used in VHDL.	**07**
		OR	
Q.4	**(a)**	Explain IF statement used in VHDL	**03**
	(b)	Describe transport delay model in brief.	**04**
	(c)	Write a VHDL code for 8 X 1 Multiplexer.	**07**
Q.5	**(a)**	Describe utility of LUT block in FPGA.	**03**
	(b)	Explain use of CLB or LAB in FPGA.	**04**
	(c)	Explain architecture of CPLD.	**07**
		OR	
Q.5	**(a)**	Discuss use of PAL blocks in CPLD.	**03**
	(b)	Explain use of PLDA for generating control signals for Power electronics application.	**04**
	(c)	Explain architecture of FPGA.	**07**

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