GUJARAT TECHNOLOGICAL UNIVERSITY
BE- SEMESTER–V (NEW) EXAMINATION – WINTER 2024

Subject Code:3154704   **Date:09-12-2024**
Subject Name:VLSI Technology and Design
Time:10:30 AM TO 01:00 PM   **Total Marks:70**
Instructions:
  1. **Attempt all questions.**
  2. **Make suitable assumptions wherever necessary.**
  3. **Figures to the right indicate full marks.**
  4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	(a)	Define Concept of Regularity, Modularity, and Locality.	03
	(b)	Compare full-custom, semi-custom and programmable VLSI design style.	04
	(c)	Explain nMOS fabrication steps using neat sketch.	07
Q.2	(a)	Draw VLSI design flow Y chart.	03
	(b)	Draw voltage transfer characteristics of ideal and practical inverter and define V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L and NM_H.	04
	(c)	Derive MOSFET current -voltage characteristics using gradual channel approximation.	07
		OR	
	(c)	Explain MOS System under External Bias with neat sketch of cross sectional view and energy band diagram and derive depletion region depth equation.	07
Q.3	(a)	What is the need of Scaling? Compare constant field and constant voltage scaling.	03
	(b)	Draw resistive load inverter. Derive V_{OL} and V_{IL} critical voltages equation of resistive load inverter.	04
	(c)	Consider resistive-load inverter with $R_L = 200$ kΩ. The enhancement-type nMOS driver transistor has the following parameters $V_{DD} = 5$ V, $V_{TO}= 0.8$V $\mu nCox = 20$ $\mu A/V^2$, W/L= 2. Determine V_{OL}, V_{IL} and NM_L.	07
		OR	
Q.3	(a)	Write VHDL program for 1-bit full adder.	03
	(b)	Draw CMOS inverter with leads name of pMOS and nMOS transistors. Derive V_{IL} critical Voltage equation of CMOS inverter	04
	(c)	Consider a CMOS inverter circuit with the following parameters: V_{DD} =3.3V, V_{TON} =0.6 V, V_{TOP}= -0.7 V, kn = 200 $\mu A/V^2$, kp = 80 $\mu A/V^2$, find the NM_L	07
Q.4	(a)	Implement following Boolean expression using CMOS inverter. Z= (A(D+E)+BC)**'**	03
	(b)	Realize following Boolean logic equation using Transmission Gate (TG). F = XY+ X'Z'+XY'Z	04
	(c)	Derive the equation for propagation delay of output signal during high to low transition of output of CMOS inverter circuit with Cload as load capacitance.	07
		OR	

Q.4	**(a)**	Draw CMOS ring oscillator and its out waveform. Write generated frequency equation.	**03**
	(b)	Construct d latch using CMOS inverters and Transmission Gates.	**04**
	(c)	Explain interconnect delay analysis using Elmore Delay model.	**07**
Q.5	**(a)**	Derive switching power dissipation equation of CMOS inverter with idea step input.	**03**
	(b)	Design CMOS SR latch circuit based on NOR gate.	**04**
	(c)	Explain MOSFET capacitance in detail.	**07**

OR

Q.5	**(a)**	Why is the size of PMOS transistor chosen to be 2.5 times of an NMOS transistor?	**03**
	(b)	Explain ASIC design flow.	**04**
	(c)	Write a short note on CMOS Transmission gate.	**07**

****