Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III (NEW) EXAMINATION – WINTER 2024

Subject Code:3130306 Date:10-12-2024

Subject Name: Fundamentals of Digital Electronics

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Subtract the following Binary numbers using 2's complement method, 1) 11010-10000 2) 11010-1101	**03**
	(b)	The message below coded in the 7-bit hamming code is transmitted through noisy channel. Decode message assuming that at most a single error occurred in code word - 0111001.	**04**
	(c)	Explain AND, OR, NOT, NAND, NOR, EX-OR and EX-NOR gate with truth table, symbol and Boolean function.	**07**
Q.2	**(a)**	Prove that A+BC = (A+B)(A+C)	**03**
	(b)	Draw AOI logic diagram of given Boolean expression $f = A + B[AC + (B + \bar{C})D]$.	**04**
	(c)	Explain Half Adder and Half Subtractor with logic diagram.	**07**
		OR	
	(c)	Explain and Design Full adder with AOI logic diagram.	**07**
Q.3	**(a)**	Expand f = A(A+B) to Maxterms and Minterms.	**03**
	(b)	Prove De morgan's theorem with the truth table.	**04**
	(c)	Find the minimal expression for $f = \sum m\{0,2,4,6,7,8,10,12,13,15\}$using K-map.	**07**
		OR	
Q.3	**(a)**	Describe 2-Input Multiplexer with logic diagram.	**03**
	(b)	Write Comparison of PLA, PAL and PROM.	**04**
	(c)	Implement the following function using 8-to-1 MUX. $f = \sum m\{0,2,3,5\}$.	**07**
Q.4	**(a)**	Explain 1-bit Magnitude Comparator with logic diagram.	**03**
	(b)	Explain 3-Line to 8-Line Decoder with logic diagram.	**04**
	(c)	Using the tabular method, obtain the minimal expression for $f = \sum m(0,1,6,7,8,9,13,14,15)$.	**07**
		OR	
Q.4	**(a)**	Draw logic diagram of Decimal to BCD Encoder.	**03**
	(b)	Design 1-Line to 4-Line Demultiplexer.	**04**
	(c)	Design 4-bit Binary to XS-3 code Converter.	**07**
Q.5	**(a)**	Draw logic diagram of 2-bit Asynchronous Ripple Down counter using Negative Edge triggered JK flip flop.	**03**
	(b)	Explain Serial IN, Parallel OUT shift register.	**04**
	(c)	Write truth table and Excitation Tables of S-R flip flop, J-K flip flop, T flip flop and D flip flop.	**07**
		OR	
Q.5	**(a)**	Explain S-R Latch.	**03**
	(b)	Explain Serial IN, Serial Out shift register.	**04**
	(c)	Design Synchronous Modulo-6 Gray code Counter with logic diagram.	**07**

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