

**GUJARAT TECHNOLOGICAL UNIVERSITY****BE - SEMESTER-III (NEW) EXAMINATION – WINTER 2023****Subject Code:3130306****Date:25-01-2024****Subject Name:Fundamentals of Digital Electronics****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

		<b>MARKS</b>
<b>Q.1</b>	(a) Subtract below binary numbers using 1's complement. $(1010)_2 - (1111)_2$	<b>03</b>
	(b) Convert Decimal number $(17)_{10}$ into Binary, Octal, Hexadecimal and BCD code.	<b>04</b>
	(c) Draw and explain symbol and truth table of AND Gate, OR Gate, NOT Gate, X-OR Gate, X-NOR Gate, NAND Gate and NOR Gate.	<b>07</b>
<b>Q.2</b>	(a) Draw and explain TTL Realization of NOT Gate.	<b>03</b>
	(b) Explain the difference between Analog and Digital system. Also explain Integrated Circuit.	<b>04</b>
	(c) Explain different Axioms and Laws of Boolean Algebra using example.	<b>07</b>
	<b>OR</b>	
	(c) Draw and explain Full Adder in detail.	<b>07</b>
<b>Q.3</b>	(a) Convert $F(A, B, C) = BC + AB$ into standard minterm form.	<b>03</b>
	(b) Minimise the logic function using Karnaugh map. $F(A, B, C, D) = \sum m(0, 1, 2, 3, 8, 9, 10, 11, 14)$ .	<b>04</b>
	(c) Draw and explain 4 bit magnitude comparator.	<b>07</b>
	<b>OR</b>	
<b>Q.3</b>	(a) Reduce the expression $F(A, B) = ((AB)' + A + AB)'$	<b>03</b>
	(b) Minimise the logic function using Karnaugh map. $F(A, B, C, D) = \sum m(0, 1, 2, 3, 8, 9, 10, 11, 14)$	<b>04</b>
	(c) Find the minimal expression for $f = \sum m(2, 8, 9, 10, 11, 12, 14)$ using tabular method.	<b>07</b>
<b>Q.4</b>	(a) Draw and explain Master-Slave Flip-Flops.	<b>03</b>
	(b) Minimise the logic function using Karnaugh map. $F(A, B, C, D) = \sum m(1, 2, 3, 8, 9, 10, 11, 14) + d(7, 15)$	<b>04</b>
	(c) Write a short note on PLA.	<b>07</b>
	<b>OR</b>	
<b>Q.4</b>	(a) Explain the difference between Combinational and sequential circuit using example.	<b>03</b>
	(b) Design a 8 to 1 multiplexer by using the four variable function given by $F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15)$ .	<b>04</b>
	(c) Draw and explain Decoder and Encoder.	<b>07</b>
<b>Q.5</b>	(a) Draw and explain SR flipflop.	<b>03</b>
	(b) Minimise the logic function using Karnaugh map. $F(A, B, C, D) = \sum (0, 2, 5, 7, 8, 10, 13, 15)$	<b>04</b>
	(c) Draw and explain Johnson counter in detail.	<b>07</b>

**OR**

- Q.5** (a) Draw and explain D Flipflop. **03**  
(b) Explain shift register. **04**  
(c) Draw the state diagram for 2 bit binary up counter and design 2 bit binary up counter using T flipflop. **07**

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