Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VII (NEW) EXAMINATION – WINTER 2021

Subject Code:3171111 Date:17/12/2021

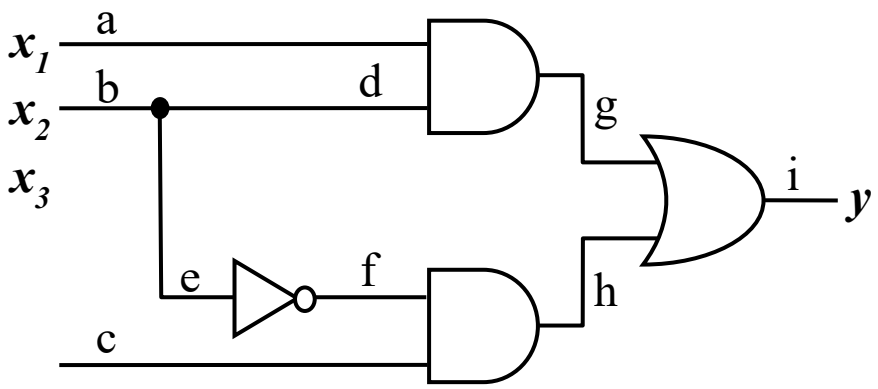
Subject Name:Testing and Verification

Time:10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Define (i) Manufacturing process yield, (ii) fault coverage and (iii) Fault detection efficiency	**03**
	(b)	Differentiate following terms: Testing and Verification	**04**
	(c)	Consider the combinational logic circuit in Figure. How many possible single stuck-at faults does this circuit have? How many collapsed single stuck at faults does this circuit have? Determine optimum input test vectors that can detect all single stuck-at faults.	**07**



Q.2	**(a)**	What is Fault modelling and its requirement?	**03**
	(b)	Discuss all the possible transistor faults in two-input CMOS NOR gate and the method of testing each of them.	**04**
	(c)	What is Mux-D scan cell design? Explain in detail. Write advantages and disadvantages of Mux-D scan cell design. Draw level-sensitive muxed-D scan cell design.	**07**
		OR	
	(c)	Explain Muxed-D full scan design architecture in detail.	**07**
Q.3	**(a)**	Define the terms: (i) Controllability (ii) Observability in context of Design for Testability	**03**
	(b)	Discuss combinational testability analysis by using necessary equations of controllability and observability of different logic gates.	**04**
	(c)	Explain partial scan design. Mention merits and demerits of partial scan design compare to full scan design.	**07**
		OR	
Q.3	**(a)**	Compare Muxed D , Cloked and LSSD scan cells	**03**
	(b)	What is scan design rule for Derived clock design style and its recommended solution?	**04**
	(c)	Draw and explain scan design flow.	**07**

Q.4	**(a)**	Differentiate fault simulation and logic simulation.	**03**
	(b)	Enlist Logic element evaluation methods. Draw input scanning algorithm. What is the value of controlling and inversion for the different logic gates?	**04**
	(c)	Draw compile code simulation flow chart and explain all the steps of compile code simulation in detail.	**07**

OR

Q.4	**(a)**	What is Functional Verification?	**03**
	(b)	Enlist different approaches of functional verification and define all.	**04**
	(c)	Explain code coverage in detail.	**07**
Q.5	**(a)**	What is function of linting tools?	**03**
	(b)	Design 4x1 multiplexer and write it test bench using any hardware description language.	**04**
	(c)	Describe simulation based verification method in detail.	**07**

OR

Q.5	**(a)**	What does 100% function coverage mean?	**03**
	(b)	What is mean by assertions in verification and explain implementation assertions and specification assertions.	**04**
	(c)	Draw serial fault simulation algorithm flow chart and explain it with an example.	**07**

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