GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER–V (NEW) EXAMINATION – WINTER 2021

Subject Code:3151105   **Date:20/12/2021**
Subject Name:VLSI Design
Time:02:30 PM TO 05:00 PM   **Total Marks: 70**
Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Explain VLSI Design flow using Y-chart	**03**
	(b)	Draw voltage transfer characteristics of inverter and define V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L and NM_H	**04**
	(c)	Derive the drain current equation for MOSFET using Gradual Channel Approximation (GCA).	**07**
Q.2	**(a)**	Compare Semi-custom and Full custom VLSI design style	**03**
	(b)	Realize following Boolean logic equation using CMOS inverter. Z= (AB+C(D+E))'	**04**
	(c)	Explain the band diagram of MOS Structure at surface inversion and derive the expression for threshold voltage.	**07**

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	(c)	Explain with net sketch diagram nMOSFET fabrication flow.	**07**
Q.3	**(a)**	Write advantages and disadvantages of dynamic logic circuit.	**03**
	(b)	Draw resistive load inverter. Derive VIL and VIH critical voltage equation of resistive load inverter.	**04**
	(c)	Design a resistive-load inverter with $R_L = 1$ kΩ, such that $V_{OL} = 0.6$ V. The enhancement-type nMOS driver transistor has the following parameters V_{DD} = 5 .0 V V_{TO}= 1. V μnCox = 22.0 μA/V² (a) Determine the required aspect ratio, W/L. (b) Determine V_{IL} and V_{IH}. (c) Determine noise margins NM_L and NM_H.	**07**

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Q.3	**(a)**	Why in symmetrical and ideal CMOS inverter required (W/L)p ≈ 2.5(W/L)n. Justify.	**03**
	(b)	Draw CMOS inverter with leads name of pMOS and nMOS transistors. Derive V_{IL} critical Voltage equation of CMOS inverter	**04**
	(c)	Consider a CMOS inverter circuit with the following parameters: V_{DD} =3.3V, V_{TON} =0.6 V, V_{TOP}= -0.7 V, kn = 200 μA/V², kp = 80 μA/V² , find the NM_L	**07**
Q.4	**(a)**	What is the need of Scaling? Mention the merits and demerits of constant field scaling.	**03**
	(b)	Draw CMOS implementation of D latch with two inverters and two CMOS TG gates.	**04**
	(c)	Draw circuit of CMOS two inputs NOR gate. Derive V_{TH} of the same.	**07**

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Q.4	**(a)**	Give comparison between FPGA and CPLD.	**03**

	(b)	Implement following Boolean logic equation using Transmission Gate (TG). Y = AB+ A'C'+AB'C	**04**
	(c)	Explain voltage bootstrapping and derive capacitance ration equation?	**07**
Q.5	**(a)**	Draw block diagram of Built in Self Test (BIST).	**03**
	(b)	Find a equivalent CMOS inverter circuit for simultaneous switching of all inputs, assume that (W/L)p = 15 for all pMOS transistors and (W/L)n = 10 for all nMOS transistors for the following Boolean equation F =[(C+D+E) . (B+A)]'	**04**
	(c)	Write a short note on CMOS Transmission gate.	**07**

OR

Q.5	**(a)**	Compare FinFET and Planner MOSFET.	**03**
	(b)	Draw NAND gate based CMOS SR latch circuit.	**04**
	(c)	Discuss the on-chip clock generation and distribution.	**07**

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