Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (OLD) EXAMINATION – WINTER 2021

Subject Code:151001 Date:03/01/2022

Subject Name:Microcontroller and Interfacing

Time:02:30 PM TO 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Describe the Flag register of 8051 with its bit significance and the function of program counter and stack pointer.	**07**
	(b)	Explain the timer operations in 8051.	**07**
Q.2	**(a)**	Explain why does the microcontrollers are known as on-chip computers?	**07**
	(b)	Discuss about status and control signals available on 8051.	**07**
		OR	
	(b)	Discuss the function of following pins: (1)EA/Vpp, (2) ALE, (3) RST, (4) XTAL1.	**07**
Q.3	**(a)**	What do you mean by key bouncing? Explain hardware and software techniques to achieve key debouncing.	**07**
	(b)	Describe IO Ports pin configurations along with suitable circuit diagram.	**07**
		OR	
Q.3	**(a)**	What do you understand by Implicit and Immediate addressing modes? Explain with suitable example. Also explain the demultiplexing of address and data buses.	**07**
	(b)	Describe how does the serial communication can be established? And also discuss the role of SCON register.	**07**
Q.4	**(a)**	Explain the interrupt sources available in 8051. Also explain IE and IP SFRs.	**07**
	(b)	Draw and explain the interfacing of 4 X 4 matrix keyboard with 8051.	**07**
		OR	
Q.4	**(a)**	Discuss the functionality of following instructions: (1) DJNZ R1, Loop, (2) MOVX A, @DPTR, (3) MOVC A, A+@DPTR	**07**
	(b)	Write a program to generate a square wave of 66% duty cycle on pin P1.5. Assume crystal frequency is 12 MHz.	**07**
Q.5	**(a)**	Explain the hardware scheme to interface ADC 0808/0809 to 8051, which reads temperature on PORT1 and Display on PORT0, where seven segment LEDs are connected.	**07**
	(b)	Write an assembly language program to transfer a block of 50 data bytes stored at D500 onwards to E500 onwards.	**07**
		OR	
Q.5	**(a)**	Discuss the hardware scheme to interface external 32K EPROM and 16K RAM memories with microcontroller.	**07**
	(b)	Two 64- bit numbers stored at locations C500 and D000, add those numbers and store the result at D500 onwards.	**07**

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