

GUJARAT TECHNOLOGICAL UNIVERSITY**BE- SEMESTER-V (NEW) EXAMINATION – WINTER 2020****Subject Code:3151105****Date:03/02/2021****Subject Name:VLSI Design****Time:10:30 AM TO 12:30 PM****Total Marks: 56****Instructions:**

1. Attempt any FOUR questions out of EIGHT questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

	MARKS
Q.1 (a) Draw CMOS inverter circuit and cross section view of nMOSFET.	03
(b) Draw voltage transfer characteristics of inverter and define V_{IL} , V_{IH} , V_{OL} , V_{OH} , NM_L and NM_H .	04
(c) Derive threshold voltage equation and explain what is substrate bias effect.	07
Q.2 (a) Realize following Boolean logic equation using CMOS inverter. $Z = (AB + C(D + E))'$	03
(b) Compare Static and Dynamic logic circuit.	04
(c) Derive drain current using gradual channel approximation.	07
Q.3 (a) Draw VTC of CMOS inverter and find operating region of NMOS and PMOS at different input voltage ranges from 0 to V_{DD} .	03
(b) Derive Critical voltages V_{IL} and V_{IH} of CMOS inverter	04
(c) Consider a CMOS inverter with the following parameters: $V_{Ton} = 0.6$ V, $V_{Top} = -0.7$ V, $K_n' = 50$ $\mu\text{A}/\text{V}^2$, $K_p' = 16$ $\mu\text{A}/\text{V}^2$, $(W/L)_n = 4$, $(W/L)_p = 5$. Calculate the noise margins of this circuit. The power supply voltage is $V_{DD} = 3.3$ V.	07
Q.4 (a) Draw resistive load inverter circuit and its VTC curve.	03
(b) Derive critical voltages V_{OH} , V_{OL} , V_{IL} and V_{IH} of resistive load inverter.	04
(c) Design resistive load inverter with following parameters: $V_{Ton} = 0.8$ V, $K_n' = 20$ $\mu\text{A}/\text{V}^2$, $(W/L)_n = 2$, $R_L = 200$ kohm and $V_{DD} = 5$ V. Calculate the noise margins of this circuit.	07
Q.5 (a) Draw transistor level circuit diagram of NOR based SR latch using CMOS.	03
(b) Derive switching power dissipation equation of CMOS inverter with idea step input.	04
(c) Justify importance of transmission gate. Realize following functions using TG. i) $F = AB + A'C' + AB'C$ and ii) $F = AB' + A'B$	07
Q.6 (a) What is need of domino CMOS logic circuit and draw it's circuit diagram.	03

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| | (b) Explain Ring oscillator | 04 |
| | (c) Draw i/p and o/p waveform during high to low transition of o/p for CMOS inverter and derive expression for τ_{PHL} using differential equation method. | 07 |
| Q.7 | (a) Draw CMOS implementation of D latch with two inverters and two CMOS TG gates. | 03 |
| | (b) Compare CPLD and FPGA. | 04 |
| | (c) Draw and Explain different clock generator and distributor circuits | 07 |
| Q.8 | (a) Compare FinFET and Planar MOSFET | 03 |
| | (b) Compare constant voltage and constant field scaling. | 04 |
| | (c) What is need of Design of Testability (DFT) in VLSI IC design and explain Built in Self Test (BIST) techniques of DFT. | 07 |
