

**GUJARAT TECHNOLOGICAL UNIVERSITY****BE - SEMESTER– III (New) EXAMINATION – WINTER 2019****Subject Code: 3132003****Date: 30/11/2019****Subject Name: Design Concepts in Basic Electronics****Time: 02:30 PM TO 05:00 PM****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

		<b>Marks</b>
<b>Q.1</b>	(a) State and explain De-Morgan's theorems.	<b>03</b>
	(b) Explain the Combination Clipper Circuits with example.	<b>04</b>
	(c) Explain with neat diagram Voltage Divider Bias.	<b>07</b>
<b>Q.2</b>	(a) Implement Full Adder using 3 to 8 Decoder.	<b>03</b>
	(b) Design 3- bit up synchronous counter.	<b>04</b>
	(c) Compare in detail RTL, DTL, TTL, ECL and CMOS.	<b>07</b>
<b>OR</b>		
<b>Q.3</b>	(c) Show that NAND and NOR are universal gate.	<b>07</b>
	(a) Explain the load line for diode.	<b>03</b>
	(b) Explain the Positive Biased Clipper Circuit with output waveform.	<b>04</b>
	(c) Make a Half and full wave Voltage Doubler Circuits and explain.	<b>07</b>
<b>OR</b>		
<b>Q.3</b>	(a) Define: (1) DC Resistance of diode, (2) Bulk Resistance and (3) PIV.	<b>03</b>
	(b) Explain the Capacitor input filter with half-wave rectifier.	<b>04</b>
	(c) Draw and Explain the working of clocked RS flip-flop.	<b>07</b>
<b>Q.4</b>	(a) Explain the ripple counter.	<b>03</b>
	(b) Draw the logic diagram and state truth table of 4x1 multiplexer.	<b>04</b>
	(c) Explain Master Slave J-K Flip Flop. List the advantages of edge triggered flip flops.	<b>07</b>
<b>OR</b>		
<b>Q.4</b>	(a) Comparison between 1's and 2's compliments.	<b>03</b>
	(b) Explain in detail bidirectional shift register with parallel load.	<b>04</b>
	(c) Explain the operation of different types of shift registers.	<b>07</b>
<b>Q.5</b>	(a) Explain the Negative Clamper circuit.	<b>03</b>
	(b) Write the difference between Half wave and Full wave Rectifier.	<b>04</b>
	(c) Drive the equation of $I_{DC}$ , $V_{DC}$ , $I_{RMS}$ , $V_{RMS}$ , Ripple Factor ( $\gamma$ ) and PIV for Half-Wave rectifier.	<b>07</b>
<b>OR</b>		
<b>Q.5</b>	(a) What are the factors affecting the stability of Q Points.	<b>03</b>
	(b) Comparison of Piecewise liner equivalent circuit, Constant Voltage Drop circuit and Ideal equivalent circuit for diode.	<b>04</b>
	(c) Explain the output Characteristics of CE Configuration for transistor with neat sketch. Also indicate different regions and explain.	<b>07</b>

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