Seat No.: _____                                        Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY
## BE - SEMESTER–VII (NEW) EXAMINATION – WINTER 2018

**Subject Code: 2170906**                                        **Date: 15/11/2018**

**Subject Name: Advanced Power Electronics**

**Time: 10:30 AM TO 01:00 PM**                                   **Total Marks: 70**

**Instructions:**
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

| | | | |
|---|---|---|---|
| **Q.1** | **(a)** | Compare buck, boost and buck-boost converter with reference to technical parameters. | **03** |
| | **(b)** | Write the advantages of resonance converter as compared to PWM converter. | **04** |
| | **(c)** | Illustrate the push pull converter with neat circuit diagram & waveform and derive the equation of output voltage in terms of input voltage & duty cycle. | **07** |
| | | | |
| **Q.2** | **(a)** | Define duty cycle and write its importance. | **03** |
| | **(b)** | Differentiate between continuous mode of conduction and discontinuous mode of conduction. | **04** |
| | **(c)** | Justify the name of converter as zero voltage switching converter with necessary diagram and waveform. | **07** |
| | | **OR** | |
| | **(c)** | Illustrate how the harmonic current are canceled by phase shifting transformer in 12 pulse rectifier. | **07** |
| | | | |
| **Q.3** | **(a)** | Compare the three topologies of multilevel inverter. | **03** |
| | **(b)** | Compare HVAC and HVDC transmission line. | **04** |
| | **(c)** | The buck-boost regulator has an input voltage = 12 V, duty cycle = 0.25, switching frequency = 25 kHz, inductor = 150 µH, filter capacitor = 220 µF and average load current = 1.25 A. Determine (a) Average output voltage (b) Peak to peak output voltage ripple (c) Peak to peak ripple current (d) Peak current of switch (e) Critical value of L and C. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Introduce the multi pulse converter. | **03** |
| | **(b)** | Draw circuit diagram of 9 level asymmetric cascaded H bridge multilevel inverter and mention the switching states to generate 0 level. | **04** |
| | **(c)** | The class E resonance inverter operates at resonance and has Vs = 12 V, R= 10 Ω, fs = 25 kHz and Q = 7. Determine  optimum value of L, C, Ce and Le. | **07** |
| | | | |
| **Q.4** | **(a)** | Draw block diagram of HVDC transmission system. Mention equipment required for HVDC system. | **03** |
| | **(b)** | Justify: ZVS is better than ZCS. | **04** |
| | **(c)** | Explain in detail about rectifier and inverter control characteristic of HVDC converter. | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | State the need of reactive power compensation. | **03** |
| | **(b)** | Draw and explain bipolar HVDC power transmission system based on 12 pulse converters for each pole. | **04** |
| | **(c)** | Discuss the operation of thyristor switched capacitor. | **07** |
| | | | |
| **Q.5** | **(a)** | Compare SVC and STATCOM. | **03** |

|   |     |                                                                                          |    |
|---|-----|------------------------------------------------------------------------------------------|----|
|   | **(b)** | Classify carrier based PWM technique for multilevel inverter. Discuss any one in detail. | **04** |
|   | **(c)** | Explain in brief about FACTS.                                                            | **07** |

**OR**

|       |         |                                                                                                    |    |
|-------|---------|----------------------------------------------------------------------------------------------------|----|
| **Q.5** | **(a)** | Explain star/delta phase shifting transformer with phasor diagram.                                 | **03** |
|       | **(b)** | Write the advantages and limitations of SSSC.                                                      | **04** |
|       | **(c)** | Explain how multilevel inverter is used as reactive power compensator with necessary vector diagram. | **07** |

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