Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V EXAMINATION – SUMMER 2025

Subject Code:3154704 Date:22-05-2025

Subject Name:VLSI Technology and Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Write 3 main differences of FPGA and CPLD.	**03**
	(b)	Draw Y chart and Flow chart of VLSI Design Flow.	**04**
	(c)	Explain Fabrication of n-MOSFET with neat sketch.	**07**
Q.2	**(a)**	Define concept of Regularity, Modularity and Locality in VLSI Design.	**03**
	(b)	Enlist different packaging technologies and explain any one.	**04**
	(c)	Explain different regions of MOS system under external bias with energy band diagram.	**07**
		OR	
	(c)	Compare Full custom, Semi custom and Fully Programmable VLSI design style.	**07**
Q.3	**(a)**	Enlist different types of MOSFET capacitance.	**03**
	(b)	Draw idea and practical inverter voltage transfer characteristics and define all critical voltages and noise margin.	**04**
	(c)	Derive drain current of MOSFET using gradual channel approximate.	**07**
		OR	
Q.3	**(a)**	What are the different small geometry effects?	**03**
	(b)	Compare different load inverters.	**04**
	(c)	Explain MOSFET Scaling and compare it.	**07**
Q.4	**(a)**	How will you calculate propagation delay times using average current method?	**03**
	(b)	Design resistive load inverter: Given V_{dd} = 5 V, k ' = 30 uA/V^2, and V_{To}= 1 V, with V_{OL}= 0.2 V. Specifically, determine the (W/L) ratio of the driver transistor and the value of the load resistor RL that achieve the required V_{OL}..	**04**
	(c)	Draw CMOS inverter. Consider a CMOS inverter with the following parameters: V_{Ton} = 0.6 V, V_{Top} = - 0.7 V ,K_n = 200 uA/V^2, K_p = 80 uA/V^2 and V_{DD} = 3.3 V. Find NM_L for a given inverter.	**07**
		OR	
Q.4	**(a)**	Define rise time, fall time and propagation delay time of CMOS inverter.	**03**
	(b)	Derive switching power dissipation equation of CMOS inverter with idea step input.	**04**
	(c)	Draw i/p and o/p waveform during high to low transition of o/p for CMOS inverter and derive expression for t_{PHL}. Using differential equation method.	**07**

Q.5	**(a)**	Implement the following Boolean function using CMOS inverter F=[(C+D+E)(B+A)]'	**03**
	(b)	Implement 2 inputs NOR and NAND gates using depletion load inverter.	**04**
	(c)	Explain CMOS Transmission gate	**07**

OR

Q.5	**(a)**	Implement NOR gate based SR latch using CMOS inverter.	**03**
	(b)	Draw CMOS implementation of D latch with two inverter and two CMOS TG gates.	**04**
	(c)	Draw ASIC design flow chart and write HDL program to implement 4x1 multiplexer using verilog hardware description language.	**07**

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