Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III EXAMINATION – SUMMER 2025

Subject Code:3130306 Date:06-06-2025

Subject Name:Fundamentals of Digital Electronics

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1*	**(a)**	Differentiate Analog and Digital system.	**03**
	(b)	Covert Hexadecimal number (1A.B) to Decimal, Binary and Octal.	**04**
	(c)	Reduce expression $F = \sum m(1, 2, 3, 4, 5, 10, 15) + d(6, 7, 12)$ using K-map and implement it using basic logic gates.	**07**
Q.2	**(a)**	Explain Error detection codes.	**03**
	(b)	Realize AND and OR gate using TTL.	**04**
	(c)	Simplify to minimal expression and implement using NAND gates: $F = W + XY[(X'Z)' + (W + Z')'Y]$	**07**
		OR	
	(c)	State and Prove De Morgan's Theorem.	**07**
Q.3	**(a)**	Explain Half adder with its implementation.	**03**
	(b)	Design full subtractor using logic gates.	**04**
	(c)	What is Code convertor? Design 4-bit binary to gray code convertor.	**07**
		OR	
Q.3	**(a)**	What is Encoder? Explain 4 to 2 Encoder.	**03**
	(b)	Design 2-bit Magnitude comparator.	**04**
	(c)	Explain Look ahead carry adder with its implementation.	**07**
Q.4	**(a)**	What is Demutiplexer? Explain 1 to 4 Demultiplexer.	**03**
	(b)	Differentiate PAL, PLA and PROM.	**04**
	(c)	Explain Mealy model of sequential circuits.	**07**
		OR	
Q.4	**(a)**	Explain functioning of RS-Flipflop.	**03**
	(b)	Give the difference between Combinational circuits and Sequential circuits.	**04**
	(c)	Implement function $F = \bar{A}B\bar{C} + A\bar{B}C$ using PAL.	**07**
Q.5	**(a)**	What is Race around condition in flip-flop? How can we avoid it?	**03**
	(b)	Describe functioning of Ring counter.	**04**
	(c)	Explain functioning of Master-slave JK-flip flop.	**07**
		OR	
Q.5	**(a)**	Give the applications of Flip-flops.	**03**
	(b)	Explain working 4-bit serial-in to parallel-out shift register.	**04**
	(c)	Implement 4-bit Asynchronous counter.	**07**

****