

**GUJARAT TECHNOLOGICAL UNIVERSITY****BE - SEMESTER-III (NEW) EXAMINATION – SUMMER 2024****Subject Code:3130306****Date:06-07-2024****Subject Name: Fundamentals of Digital Electronics****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

- Q.1** (a) Subtract the following Binary numbers using 1's complement method, **03**  
 1) 110111-10000 2) 11010-11011
- (b) Write given Binary number 1101 into the 7-bit hamming code. **04**
- (c) Draw and explain TTL Realization of AND, OR, NOT Gate. **07**
- Q.2** (a) Draw the symbols and truth tables of AND, OR and NOT Gate. **03**
- (b) Draw AOI logic diagram of given Boolean expression **04**  
 $f = A + B[\bar{A} + (B + \bar{C})D]$ .
- (c) Explain Half Adder and Half Subtractor with logic diagram. **07**
- OR**
- (c) Explain and Design Full Subtractor with AOI logic diagram. **07**
- Q.3** (a) Expand  $f = AC+AB$  to maxterms and minterms. **03**
- (b) Prove De morgan's theorem with the truth table. **04**
- (c) Minimise the logic function  $F(A,B,C,D) = \Pi M(1, 2, 3, 8, 9, 10, 11,14) \cdot d$  **07**  
 (7, 15) Use Karnaugh map. Draw the logic circuit for the simplified function using NOR gates only.
- OR**
- Q.3** (a) Draw logic diagram of Octal to Binary Encoder. **03**
- (b) Explain Axioms and Laws of Boolean algebra. **04**
- (c) Implement the following function using 8-to-1 MUX.  $f = \sum m\{0,1,4,6\}$  **07**
- Q.4** (a) Write Comparison of PLA, PAL and PROM. **03**
- (b) Explain 3-Line to 8-Line Decoder with logic diagram. **04**
- (c) Draw and explain 3 bit magnitude comparator. **07**
- OR**
- Q.4** (a) Explain Serial IN, Serial OUT shift register. **03**
- (b) Design 1-Line to 4-Line Demultiplexer. **04**
- (c) Design and Implement 4-bit XS-3 to Binary code Converter. **07**
- Q.5** (a) Explain S-R Master-slave flip flop. **03**
- (b) Design and Implement 3 bit binary to Gray code converter. **04**
- (c) Write truth table and Excitation Tables of S-R flip flop, J-K flip flop, T flip flop and D flip flop. **07**
- OR**
- Q.5** (a) Explain J-K flip flop with logic diagram. **03**
- (b) Design 2 bit ripple UP asynchronous counter using negative edge triggering of flip flop. **04**
- (c) Design and Implement Synchronous 3 bit UP/DOWN Counter using J-K Flip flop. **07**

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