GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER–III(NEW) EXAMINATION – SUMMER 2023

Subject Code:3132003   **Date:28-07-2023**
Subject Name:Design Concepts in Basic Electronics
Time:02:30 PM TO 05:00 PM   **Total Marks:70**

Instructions:
1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

Q.1	**(a)**	Briefly explain analog system and digital system.	**03**
	(b)	What are the advantages of digital system?	**04**
	(c)	What is emitter feedback bias for transistor? Explain in detail.	**07**
Q.2	**(a)**	Explain the choke input filter.	**03**
	(b)	Explain Gray Code with one application.	**04**
	(c)	Explain NAND Gate as universal Gate.	**07**
		OR	
	(c)	Explain RTL, DTL and TTL in detail.	**07**
Q.3	**(a)**	Convert $(B9A2)_{16}$ to its equivalent binary number and Convert $(539)_{10}$ to its equivalent BCD number.	**03**
	(b)	Perform $(1101)_2 \times (1010)_2$ and $(1100)_2 \div (100)_2$ with proper steps.	**04**
	(c)	Explain AND, OR and NOT Gates in detail with their discrete circuits.	**07**
		OR	
Q.3	**(a)**	What is Q-point of a transistor?	**03**
	(b)	Explain intrinsic and extrinsic semiconductor materials.	**04**
	(c)	Explain positive clamper and negative clamper circuits with bias.	**07**
Q.4	**(a)**	Reduce the following Boolean expression to its simplest form and implement the circuit using minimum number of Gates. **[AB'(C+BD)+A'B']C**	**03**
	(b)	Explain serial in serial/serial out shift register.	**04**
	(c)	Simplify the following function using Karnaugh map method. Also implement the circuit for minimized function using logic gates. $F (A, B, C, D) = \sum\{0,1,4,5,6,7,9,11\}$	**07**
		OR	
Q.4	**(a)**	Explain any one voltage multiplier circuit.	**03**
	(b)	Explain input output characteristics for common emitter configuration of transistor.	**04**
	(c)	Design and explain Asynchronous up-down counter.	**07**
Q.5	**(a)**	Explain half wave rectifier circuit with waveforms.	**03**
	(b)	Explain series clipper circuits with waveforms.	**04**
	(c)	Explain V-I Characteristics of PN Junction diode.	**07**
		OR	
Q.5	**(a)**	Explain 1×4 Demultiplexer.	**03**
	(b)	Explain Gated S-R Latch with wave forms.	**04**
	(c)	Design full adder and full subtracter combinational circuits.	**07**

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