Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III (NEW) EXAMINATION – SUMMER 2022

Subject Code:3131704 Date:11-07-2022

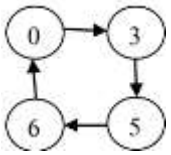
Subject Name:Digital Electronics

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	What do you mean by universal gates? Implement NOT, AND, OR with any one universal gate.	**03**
	(b)	Explain De Morgan's theorem and associative law with suitable example.	**04**
	(c)	Design 3 – bit Gray code to binary code converter.	**07**
Q.2	**(a)**	Define the following: 1) Noise Margin 2) Propagation Delay 3) Fan IN-Fan OUT	**03**
	(b)	Expand A+BC'+ABD'+ABCD to min terms and max terms.	**04**
	(c)	Reduce using mapping the expression Σ m(0,1,2,3,5,7,8,9,10,12,13) using K-map and implement it with NAND gate.	**07**
		OR	
	(c)	Minimize and implement the following output functions using K-map F1=Σ m(1,2,3,6,8,12,14,15) F2=Π M(3,4,5,7,11,13,15)+D(6,8)	**07**
Q.3	**(a)**	Reduce the expression (B+BC)(B+B'C)(B+D)=B	**03**
	(b)	With neat sketch explain the operation of clocked RS flip flop with NAND and NOR gates.	**04**
	(c)	Design two bit magnitude comparator with necessary diagram and equations.	**07**
		OR	
Q.3	**(a)**	Explain transistor transistor logic for NAND gate.	**03**
	(b)	Explain half and full adder with necessary diagram and truth table.	**04**
	(c)	Explain master and slave flip flop with necessary diagram.	**07**
Q.4	**(a)**	How does an encoder differ from a decoder?	**03**
	(b)	Explain BUS transfer logic for two registers.	**04**
	(c)	Design a type T counter for given state diagram.	**07**



OR

Q.4	**(a)**	Differentiate between sequential logic and combinatorial logic.	**03**
	(b)	Explain arithmetic and logic micro operation.	**04**
	(c)	Explain 2 bit up counter using JK flip flop with K-map equations and circuit diagram.	**07**
Q.5	**(a)**	Explain 4 *1 multiplexer with diagram and truth table.	**03**
	(b)	Derive JK and D flip-flop excitation tables from their truth tables.	**04**

	(c)	Minimize the following function using tabulation method: $F(w, x, y, z) = \sum (0,1,2,8,10,11,14,15)$	**07**

OR

Q.5	**(a)**	Write a note on ALU.	**03**
	(b)	Explain BCD adder with diagram and truth table.	**04**
	(c)	List out different types of memories used in digital logic circuits and define them.	**07**

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