Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (NEW) EXAMINATION – SUMMER 2021

Subject Code:3151105 Date:17/09/2021

Subject Name:VLSI Design

Time:10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Describe: (1) Regularity (2) Modularity (3) Locality	**03**
	(b)	Differentiate Full Custom and Semi Custom Design flow	**04**
	(c)	Describe VLSI Design Flow.	**07**
Q.2	**(a)**	Describe process of photo lithography with example.	**03**
	(b)	Describe FPGA Architecture.	**04**
	(c)	Sketch PMOS fabrication steps	**07**
		OR	
	(c)	Describe device isolation techniques with example.	**07**
Q.3	**(a)**	Derive equation for depletion depth for inversion region of two terminal MOS structure.	**03**
	(b)	Sketch Resistive load NMOS inverter circuit and its VTC. Derive equation of V_{OL}	**04**
	(c)	Describe Gradual Channel Approximation and Derive equation for drain current.	**07**
		OR	
Q.3	**(a)**	For NMOS transistor, gate voltage is 2v, drain voltage is 5v, source is connected to ground and threshold voltage is 1v. Find operating region of NMOS and drain current. ($Kn = 60\ \mu A/V^2$)	**03**
	(b)	Sketch CMOS inveter circuit and its VTC. Describe various regions of VTC. Derive equation for Vth.	**04**
	(c)	What is Scaling? Describe voltage scaling and derive necessary parameter.	**07**
Q.4	**(a)**	Define: τ_{PHL}, τ_{PLH}, τ_{rise} with necessary diagram.	**03**
	(b)	Sketch and Describe D-Latch circuit using CMOS-Transmission Gate(TG).	**04**
	(c)	Why does NMOS pass strong logic-0 and weak logic-1?	**07**
		OR	
Q.4	**(a)**	Describe CMOS ring oscillator	**03**
	(b)	Sketch static CMOS circuit for following Boolean equation. F1 = X'Y + XY' F2 = AB(C+D)	**04**
	(c)	Describe basic dynamic CMOS logic concept.	**07**
Q.5	**(a)**	Describe FinFET Structure with neat diagram.	**03**

	(b)	Describe Latch-up problem in IC.	**04**
	(c)	Describe different types of fault.	**07**
		OR	
Q.5	**(a)**	Compare FinFET and MOSFET.	**03**
	(b)	Describe methods for on-chip clock generation.	**04**
	(c)	Describe Ad-Hoc Testable design technique.	**07**

****