GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER–III (NEW) EXAMINATION – SUMMER 2021

Subject Code:3131704   **Date:06/09/2021**
Subject Name:Digital Electronics
Time:10:30 AM TO 01:00 PM   **Total Marks:70**
Instructions:
        1. **Attempt all questions.**
        2. **Make suitable assumptions wherever necessary.**
        3. **Figures to the right indicate full marks.**
        4. **Simple and non-programmable scientific calculators are allowed.**
           .   **MARKS**

Q.1	**(a)**	1. Give logic diagram and truth-table of EX-OR Gate 2. Subtract $(3250-72532)_{10}$ using 10s compliment 3. F= x y + x' y' + y' z implement with gates	**03**
	(b)	Define : 1) Fan in 2) Fan out 3) Propagation Delay 4) Noise margin	**04**
	(c)	Design the full adder and full subtractor	**07**
Q.2	**(a)**	Covert to another canonical form 1. $F(A,B,C)=\sum(1,7)$ 2. $F(W,X,Y,Z)=\Pi(1,2,5,15)$ 3. $F(a,b,c,d,e)=\sum(1,2,7,8,9,10,11,13,14,23)$	**03**
	(b)	State and prove De Morgan's Law. Find the complement of $F(A,B,C)=\sum(1,7)$	**04**
	(c)	Design 3 – bit Gray code to binary code converter.	**07**

<div align="center">OR</div>

	(c)	Draw the logic diagram of 3:8 Decoder and write the truth table. Explain its operation.	**07**
Q.3	**(a)**	Simplify: A'B + A'BC' + A'BCD + A'BC'D'E	**03**
	(b)	Implement the following Boolean function F= (A + B′) (CD + E) with NAND gates	**04**
	(c)	List the characteristics of Logic families. Explain DTL logic family in brief	**07**

<div align="center">OR</div>

Q.3	**(a)**	Explain combinational logic circuit and sequential logic circuit	**03**
	(b)	Reduce using K-mapping the expression F = Σ(1,5,6,12,13,14)+d(2,4) where d is don't care condition. Find out SOP	**04**
	(c)	Simplify the Boolean function using the tabulation method $F(A,B,C,D,E,F,G)=\sum(20,28,38,39,52,60,102,103,127)$	**07**
Q.4	**(a)**	Explain the operation of master slave J-K flip flop	**03**
	(b)	Write the note on SR and JK Flip Flop	**04**
	(c)	Simplify the following Boolean function F(A,B,C,D) =Σ(0,1,2,5,8,9,10).Implement the simplified equation using NAND gates only	**07**

<div align="center">OR</div>

Q.4	**(a)**	Explain the working of 3-bit Ring counter with necessary diagram using negative edge triggered D flip - flop.	**03**
	(b)	Design a combinational circuit that will detect identical bits for 2 bit number	**04**
	(c)	Explain BCD Ripple counter and draw its logic diagram and timing diagram	**07**

Q.5	**(a)**	Write a note on ALU	**03**
	(b)	Explain arithmetic, logic and shift micro operation	**04**
	(c)	Design a counter using D-flip flop, having the state diagram as	**07**

OR

Q.5	**(a)**	Realize Ex-OR gate and NOT gate using NOR gate.	**03**
	(b)	Explain state table, state diagram with example.	**04**
	(c)	Explain 4 bit magnitude comparator with necessary Boolean expression.	**07**

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