Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – SUMMER 2019

Subject Code: 2130306 Date: 18/06/2019

Subject Name:Fundamentals of Digital Design

Time: 02:30 PM TO 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Perform BCD subtraction using 9's complement for : $(151.6 - 89.7)_{10}$	**03**
	(b)	Draw logic symbols for Bubbled-AND & NOR gate. Prove that both give same output using truth table.	**04**
	(c)	Draw AOI logic for (A'B + AB') and convert it to NAND and NOR logic.	**07**
Q.2	**(a)**	Which are called Universal Logic Gates? Explain with one example why?	**03**
	(b)	Expand A(B' + A)B to maxterms and minterms.	**04**
	(c)	Reduce the following expression using K-map and implement it in universal logic: Σ m(0, 1, 2, 3, 4, 6, 8, 9, 10, 11)	**07**
		OR	
	(c)	Minimize the following expression using tabulation method: Σ m(0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)	**07**
Q.3	**(a)**	Explain Half-subtractor in detail with equations and NOR logic circuit.	**03**
	(b)	Explain 4x1 multiplexer in detail.	**04**
	(c)	Design 2-bit parallel adder using Look-Ahead Carry.	**07**
		OR	
Q.3	**(a)**	Explain Half-adder in detail with equations and NAND logic circuit.	**03**
	(b)	Explain 4-bit ripple adder with block diagram.	**04**
	(c)	Design a combination circuit where input given at D_1 of 2x1 multiplexer can be displayed at D_3 output of 1x4 demutiplexer.	**07**
Q.4	**(a)**	What are Active-High and Active-Low configurations? Explain in detail.	**03**
	(b)	Explain edge triggered D Flip flop.	**04**
	(c)	Explain NAND gate S-R latch and NOR Gate S-R latch with truth table and Logic circuit.	**07**
		OR	
Q.4	**(a)**	List different applications of Flip-Flops.	**03**
	(b)	Explain edge triggered T Flip flop.	**04**
	(c)	Explain edge triggered JK Flip-flop for Active-High and Active-Low configuration.	**07**
Q.5	**(a)**	For DAC define: (1) Resolution, (2)Settling time (3) Offset Voltage	**03**
	(b)	Explain Programmable Array Logic (PAL) with basic circuit structure.	**04**
	(c)	Explain Serial-IN Serial-OUT shift register.	**07**

OR

Q.5	**(a)**	List types of A/D convertors.	**03**
	(b)	Using simplified connection method in PLA circuits draw circuit for following functions: $F_1 = AB'C + A'B'C + AC$ $F_2 = ABC + AB' + C$	**04**
	(c)	Explain BCD to Seven Segment decoder for common-cathode LED display.	**07**

****